

# TS-QS8LL314H40PC

## 400G-ER8 QSFP-DD Transceiver

### Features:

- Compliant with IEEE std 802.3cnTM-2019:
- 400GBASE-ER8 optical interface
- 400GAUI-8 electrical interface
- Compliant with QSFP-DD MSA HW Rev 5.0 with duplex LC connector
- Compliant with QSFP-DD CMIS Rev 4.0
- Case operating temperature 0°C to 70°C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive 2011/65/EU (RoHS compliant)
- Class 1/1M Laser

### Module Characteristics

**Table 1 – Absolute Maximum Ratings**

Parameter	Symbol	Min.	Max.	Unit	Notes
Storage Temperature	TS	-40	85	°C	
Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Data Input Voltage Differential	IVDIP-VDINI	-	1	V	
Control Input Voltage	VI	-0.3	VCC+0.5	V	
Control Output Current	IO	-20	20	mA	

**Table 2 – Recommended Operating Conditions**

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	TOPR	0	-	70	°C	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	ICC_IP	-	-	5200	mA	
Sustained peak current at hot plug	ICC_SP	-	-	4290	mA	
Maximum Power Dissipation	PD	-	-	13	W	
Maximum Power Dissipation, Low Power Mode	PDLP	-	-	1.5	W	
Signalling Speed per Lane	DRL	-	26.5625	-	GBd	

Control Input Voltage High	V <sub>IH</sub>	VCC*0.7	-	VCC+0.3	V	
Control Input Voltage Low	V <sub>IL</sub>	-0.3	-	VCC*0.3	V	
Two Wire Serial Interface Clock Rate	-	-	-	400	kHz	
Power Supply Noise	-	-	-	66	mVpp	
Rx Differential Data Output Load	-	-	100	-	Ohm	
Operating Distance	-	0.002	-	40(30)	km	1

Note 1: Channel insertion loss is 18dB for 40km and 15dB for 30km.

## Functional Characteristics (Optical)

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

**Table 3 – Transmitter Optical Specifications**

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0	$\lambda C0$	1272.55	1273.55	1274.54	nm	
Wavelength L1	$\lambda C1$	1276.89	1277.89	1278.89	nm	
Wavelength L2	$\lambda C2$	1281.25	1282.26	1283.27	nm	
Wavelength L3	$\lambda C3$	1285.65	1286.67	1287.68	nm	
Wavelength L4	$\lambda C4$	1294.53	1295.56	1296.59	nm	
Wavelength L5	$\lambda C5$	1299.02	1300.06	1301.09	nm	
Wavelength L6	$\lambda C6$	1303.54	1304.59	1305.63	nm	
Wavelength L7	$\lambda C7$	1308.09	1309.14	1310.19	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Total Average Launch Power	AOPT	-	-	14.6	dBm	
Average Launch Power, each lane	AOPL	-0.6	-	5.6	dBm	1
Outer Optical Modulation Amplitude (OMA <sub>outer</sub> ), each Lane, 40km	TOMA	2.4	-	6.4	dBm	
Outer Optical Modulation Amplitude (OMA <sub>outer</sub> ), each Lane, 30km	TOMA	0.4	-	4.4	dBm	
Difference in Launch Power between any two Lanes (OMA <sub>outer</sub> )	DT_OMA	-	-	4	dB	
Launch Power in OMA <sub>outer</sub> minus TDECQ, each lane, 40km	TOMA-TDECQ	1	-	-	dBm	
Launch Power in OMA <sub>outer</sub> minus TDECQ, each lane, 30km	TOMA-TDECQ	-1	-	-	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ	-	-	3.4	dB	

Average Launch Power of OFF Transmitter, each lane	TOFF	-	-	-30	dBm	
Extinction Ratio	ER	6	-	-	dB	
RIN15OMA	RIN	-	-	-132	dB/Hz	
Optical Return Loss Tolerance	ORL	-	-	15	dB	
Transmitter Reflectance	TR	-	-	-26	dB	2

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength

Note 2: Transmitter reflectance is defined looking into the transmitter

**Table 4 – Receiver Optical Specifications**

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Wavelength L0	$\lambda C0$	1272.55	1273.55	1274.54	nm	
Wavelength L1	$\lambda C1$	1276.89	1277.89	1278.89	nm	
Wavelength L2	$\lambda C2$	1281.25	1282.26	1283.27	nm	
Wavelength L3	$\lambda C3$	1285.65	1286.67	1287.68	nm	
Wavelength L4	$\lambda C4$	1294.53	1295.56	1296.59	nm	
Wavelength L5	$\lambda C5$	1299.02	1300.06	1301.09	nm	
Wavelength L6	$\lambda C6$	1303.54	1304.59	1305.63	nm	
Wavelength L7	$\lambda C7$	1308.09	1309.14	1310.19	nm	
Damage Threshold, each Lane	AOPD	-3.4	-	-	dBm	
Average Receive Power, each Lane	AOPR	-18.6	-	-4.4	dBm	
Receive Power (OMAouter), each Lane	OMAR	-	-	-3.6	dBm	
Difference in Receive Power between any two Lanes (OMAouter)	DR_OMA	-	-	5.8	dB	
Receiver Reflectance	RR	-	-	-26	dB	
Receiver Sensitivity (OMAouter), each Lane, 40km	SOMA	-	-	-16.1	dBm	1
Receiver Sensitivity (OMAouter), each Lane, 30km	SOMA	-	-	-15.1	dBm	1
Stressed Receiver Sensitivity (OMAouter), each Lane, 40km	SRS	-	-	-14.1	dBm	2
Stressed Receiver Sensitivity (OMAouter), each Lane, 30km	SRS	-	-	-13.1	dBm	2

Note 1: Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with SECQ of 1.4 dB.

Note 2: Measured with conformance test signal at TP3 for the BER = 2.4x10<sup>-4</sup>

## Functional Characteristics (Electrical)

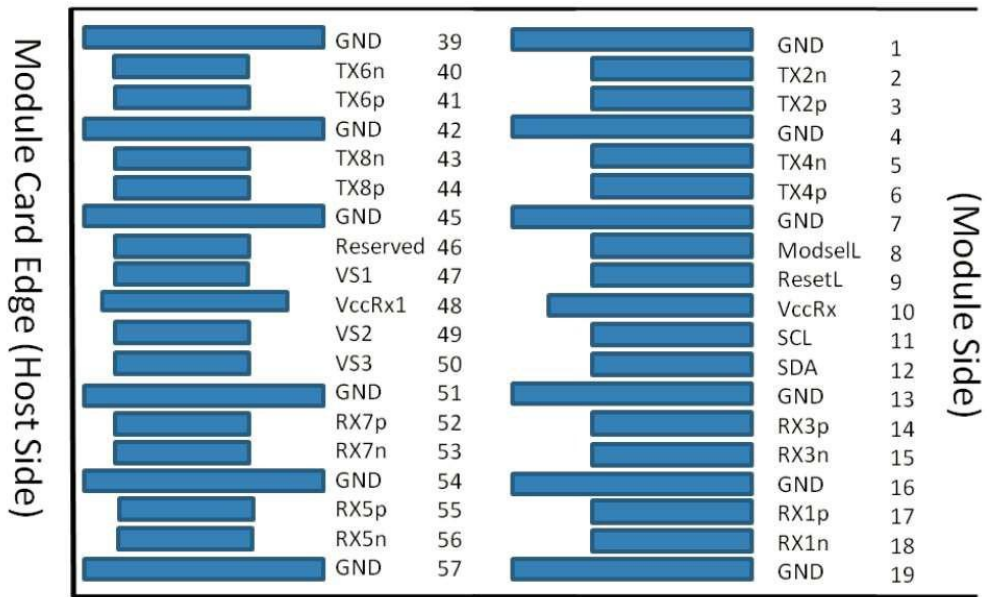
**Table 5 – Electrical Specification High Speed Signal (compliant with IEEE 802.3 400GAUI-8)**

<b>Receiver (Module Output)</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Min.</b>	<b>Typical</b>	<b>Max.</b>	<b>Unit</b>	<b>Notes</b>
AC common-mode output Voltage (RMS)		-	-	17.5	mV	
Differential output Voltage		-	-	900	mV	
Near-end Eye height, differential		70	-	-	UI	
Far-end Eye height, differential		30	-	-	UI	
Far end pre-cursor ratio		-	-	2.5	%	
Differential Termination Mismatch		-	-	10	%	
Transition Time (min, 20% to 80%)		9.5	-	-	ps	
DC common mode Voltage		-350	-	2850	mV	
<b>Transmitter (Module Input)</b>						
<b>Parameter</b>	<b>Symbol</b>	<b>Min.</b>	<b>Typical</b>	<b>Max.</b>	<b>Unit</b>	<b>Notes</b>
Differential pk-pk input Voltage tolerance		900	-	-	mV	
Differential termination mismatch		-	-	10	%	
Single-ended voltage tolerance range		-0.4	-	3.3	V	
DC common mode Voltage		-350	-	2850	mV	

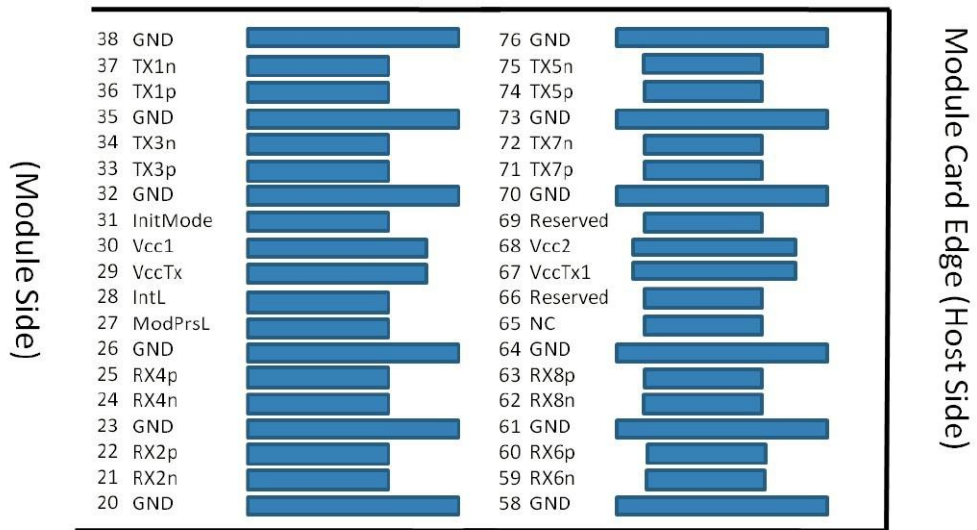
**Table 6 – Electrical Specification Low Speed Signal (compliant with QSFP-DD HW Rev 5.0)**

<b>Parameter</b>	<b>Symbol</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>	<b>Condition</b>
Module output SCL and SDA	VOL	0	0.4	V	
	VIL	-0.3	VCC*0.3	V	
Module Input SCL and SDA	VIH	VCC*0.7	VCC+0.5	V	
	VIL	-0.3	0.8	V	
InitMode, ResetL and ModSelL	VIH	2	VCC+0.3	V	
	VOL	0	0.4	V	
IntL	VOH	VCC-0.5	VCC+0.3	V	

## Pin Definitions



Bottom side viewed from bottom



Top side viewed from top

Figure 1 – Pin definitions of the module high speed inputs/outputs

**Table 7 – Module Pin Definitions**

Pin #	Logic	Symbol	Definition	Pin #	Logic	Symbol	Definition
1		GND	Ground	39		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input	40	CML-I	Tx6n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	41	CML-I	Tx6p	Transmitter Non-inverted Data Input
4		GND	Ground	42		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input	43	CML-I	Tx8n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	44	CML-I	Tx8p	Transmitter Non-inverted Data Input
7		GND	Ground	45		GND	Ground
8	LVTTL-I	ModSelL	Module Select	46		Reserved	
9	LVTTL-I	ResetL	Module Reset	47		VS1	Module Vendor Specific 1
10		VccRx	+3.3V Power Supply Receiver	48		VccRx1	3.3V Power Supply
11	LVCMS-I/O	SCL	2-wire serial interface clock	49		VS2	Module Vendor Specific 2
12	LVCMS-I/O	SDA	2-wire serial interface data	50		VS3	Module Vendor Specific 3
13		GND	Ground	51		GND	Ground
14	CML-O	Rx3p	Receiver Non-inverted Data Output	52	CML-O	Rx7p	Receiver Non-inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output	53	CML-O	Rx7n	Receiver Inverted Data Output
16		GND	Ground	54		GND	Ground
17	CML-O	Rx1p	Receiver Non-inverted Data Output	55	CML-O	Rx5p	Receiver Non-inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output	56	CML-O	Rx5n	Receiver Inverted Data Output
19		GND	Ground	57		GND	Ground
20		GND	Ground	58		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output	59	CML-O	Rx6n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-inverted Data Output	60	CML-O	Rx6p	Receiver Non-inverted Data Output
23		GND	Ground	61		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output	62	CML-O	Rx8n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-inverted Data Output	63	CML-O	Rx8p	Receiver Non-inverted Data Output
26		GND	Ground	64		GND	Ground
27	LVTTL-O	ModPrsL	Module Present	65		NC	Not connected
28	LVTTL-O	IntL	Interrupt	66		Reserved	
29		VccTx	+3.3V Power Supply	67		VccTx1	3.3V Power Supply

		Transmitter					
30		Vcc1	+3.3V Power Supply	68	Vcc2	3.3V Power Supply	
31	LVTTL-I	InitMode	Initialization mode	69	Reserved		
32		GND	Ground	70	GND	Ground	
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	71	CML-I	Tx7p	Transmitter Non-inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input	72	CML-I	Tx7n	Transmitter Inverted Data Input
35		GND	Ground	73	GND	Ground	
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	74	CML-I	Tx5p	Transmitter Non-inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input	75	CML-I	Tx5n	Transmitter Inverted Data Input
38		GND	Ground	76	GND	Ground	

### Recommended QSFP-DD Host Board Schematic

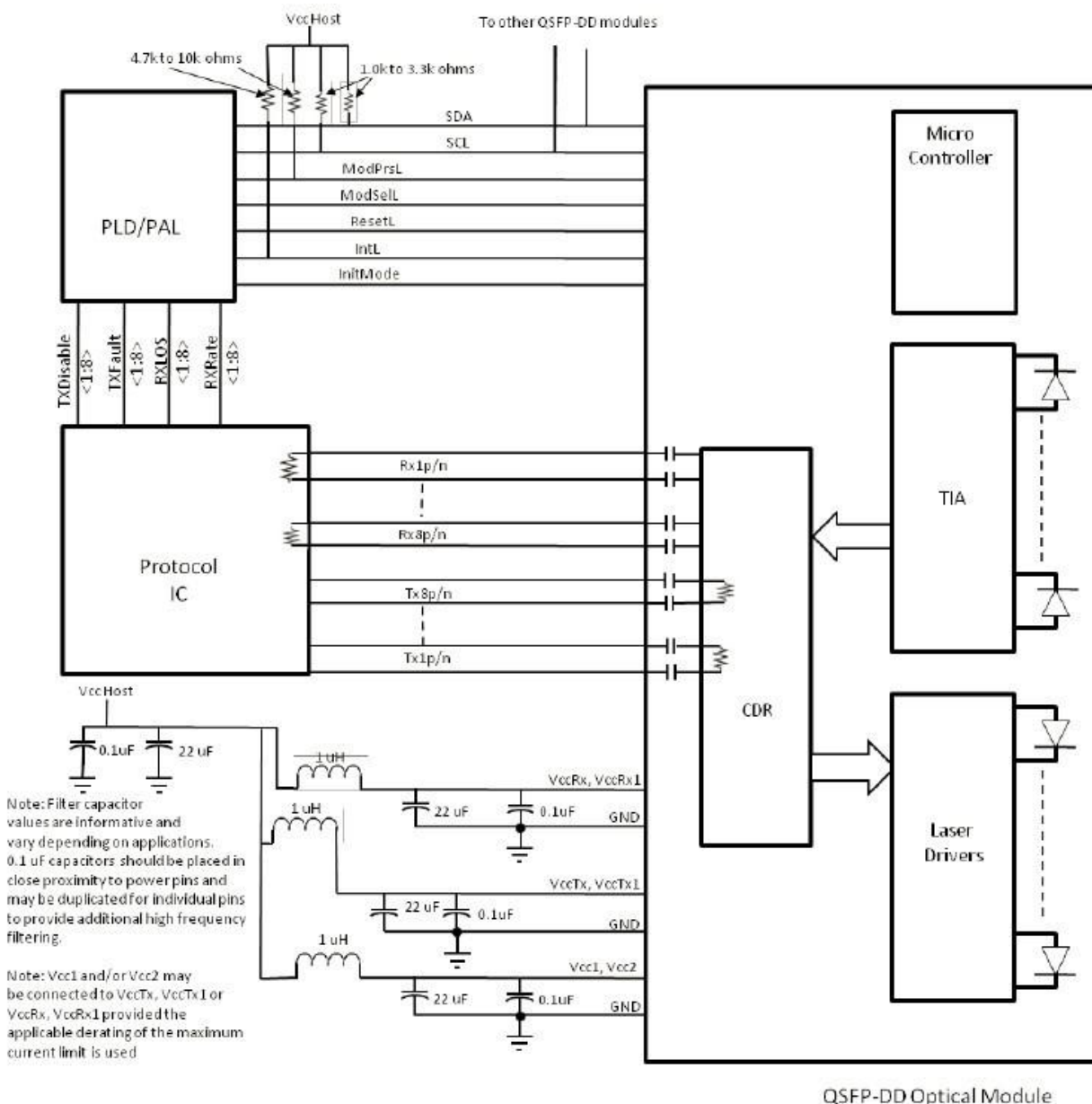


Figure 2 – Recommended QSFP-DD Host Board Schematic

**Table 8 – Timing for Soft Control and Status Functions**

Parameter	Symbol	Min.	Max.	Unit	Notes
MgmtInit Duration		-	2000	ms	
ResetL Assert Time	t_reset_init	10	-	μs	
IntL Assert Time	ton_IntL	-	200	ms	
IntL Deassert Time	toff_IntL	-	500	μs	
Rx LOS Assert Time (fast mode)	ton_losf	-	1	ms	
Rx LOS Deassert Time (fast mode)	toff_losf	-	3	ms	
Tx Fault Assert Time	ton_Txfault	-	200	ms	
Flag Assert Time	ton_flag	-	200	ms	
Mask Assert Time	ton_mask	-	100	ms	
Mask Deassert Time	toff_mask	-	100	ms	
Module Select Wait Time	ModSelL Wait Time	-	N/A		Note

Note: This feature is not supported

**Table 9 – I/O Timing for Squelch and Disable**

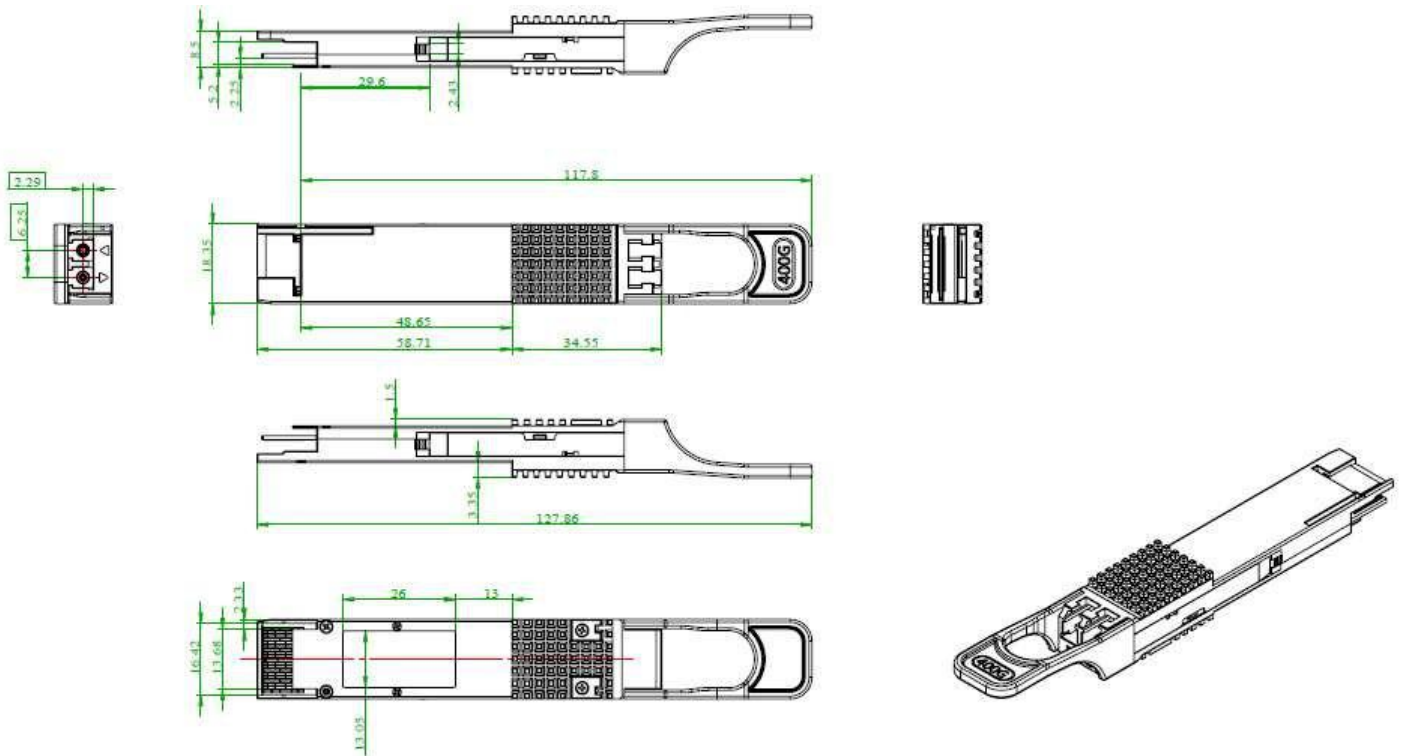
Parameter	Symbol	Min.	Max.	Unit	Notes
Rx Squelch Assert Time	ton_Rxsq	-	15	ms	
Rx Squelch Deassert Time	toff_Rxsq	-	1500	ms	
Tx Squelch Assert Time	ton_Txsq	-	400	ms	
Tx Squelch Deassert Time	toff_Txsq	-	1500	ms	Based on modulation
Tx Disable Assert Time (fast mode)	ton_Txdisf	-	3	ms	
Tx Disable Deassert Time (fast mode)	toff_Txdisf	-	10	ms	
Rx Output Disable Assert Time	ton_Rxdis	-	100	ms	
Rx Output Disable Deassert Time	toff_Rxdis	-	100	ms	
Squelch Disable Assert Time	ton_sqdis	-	N/A	ms	Not support
Squelch Disable Deassert Time	toff_sqdis	-	N/A	ms	Not support

**Table 10 – Digital Diagnostics**

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to VCC	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-0.6 to +5.6	±3	dB	Internal
Rx Receive Power (Each Lane)	-18.6 to -4.4	±3	dB	Internal

## Mechanical Diagram





## Ordering Information

Table 11 - Ordering Information

Part No.	Application	Data Rate	Laser Source	Distance
TS-S8LL314H40PC	400GBASE-ER8	400GB Ethernet	EML	40km
TS-S8LL314H30PC	400GBASE-ER8L	400GB Ethernet	EML	30km

## Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: Radiation emitted by laser devices can be dangerous to human eyes. Avoid eye exposure to direct or indirect radiation.

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