TS-QS4LL292H40PC
200G QSFP-DD ER4

Features

- Supports 200GBASE-ER4;
- Lane bit rate 53.125 Gb/s with PAM4;
- Up to 40km transmission on SMF;
- LAN WDM EML laser and APD receiver;
- 200GAUI-8 Electrical interface with 8 Lanes 26.5625Gb/s NRZ high-speed signal;
- I2C interface with integrated Digital Diagnostic monitoring;
- QSFP-DD MSA package with duplex LC connector;
- Compliant with IEEE 802.3cn 200GBASE-ER4
- Single +3.3V power supply;
- Maximum power consumption 10W;
- Operating case temperature: 0 to +70 °C;
- Compliant to QSFP-DD CMIS standard;
- Compliant to 802.3cu& QSFP-DD MSA HW standard;
- Complies with EU Directive 2015/863/EU;

Application

- 200GBASE-ER4 Ethernet (PAM4)
- 5G Back-haul
- Data center
- Cloud application.

Order Information

Table 1- order information

Part No.	Data Rate	Laser	Fiber Type	Distance	Optical Interface	Temp	DDMI
TS-QS4LL292H40PC	212.5Gb/s	LANWDM	SMF	40km	LC	0~70C	Y

Absolute Maximum Ratings

Table 2-Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	T_S	-40	-	85	°C
Supply Voltage	V_{CC}	-0.5	-	3.6	V
Operating Relative Humidity	RH	5	-	85	%

Recommended Operating Conditions

Table 3-Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Case Temperature	T_C	0	-	70	°C	
Power Supply Voltage	V_{CC}	3.13	3.3	3.47	V	
Power Dissipation	P	-	-	10	W	
Aggregate Bit Rate	BRAVE	-	212.5	-	Gb/s	With PAM4

Lane Bit Rate	BRLANE	-	53.125	-	Gb/s	With PAM4
Transmission Distance	TD	-	-	40	km	Over SMF

Optical Characteristics

Table 4-Optical Characteristics

Transmitter						
Parameter	**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**	**Notes**
Signaling rate, each lane	BR	26.5625 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Side-mode suppression ratio	SMSR	30	-	-	dB	
Total average launch power	P_{MAX}	-	-	12.6	dBm	SMF
Average launch power, each lane	P_{OUT}	0.4	-	6.6	dBm	SMF
Outer OMA, each lane	OMA_{outer}	3.4	-	7.4	dBm	SMF
Difference in launch power between lanes		-	-	4	dB	OMA
Launch power in OMA_{outer} minus TDECQ	OMA_{outer} - TDECQ	2	-	-	dBm	ER≥ 4.5dB
Transmitter and dispersion eye closure for PAM4	TDECQ	-	-	3.2	dB	
Average POUT (Laser Turn off)	P_{OFF}	-	-	-30	dBm	
Extinction ratio, each lane	ER	6	-	-	dB	
Receiver						
Signaling rate, each lane	BR	26.5625 ± 100 ppm			GBd	
Modulation format		PAM4				
Lane wavelengths	L0	1294.53	1295.56	1296.59	nm	
	L1	1299.02	1300.05	1301.09	nm	
	L2	1303.54	1304.58	1305.63	nm	
	L3	1308.09	1309.14	1310.19	nm	
Damage threshold, each lane	P_{DAMAGE}	-2.4	-	-	dBm	
Average receive power, each lane	P_{RX_LANE}	-17.6	-	-3.4	dBm	
Receive power (OMA_{outer}), each lane	RX_{OMA}	-	-	-2.6	dBm	
Receiver sensitivity (OMA_{outer}), each lane	SEN_{OMA}	-	-	-15.1	dBm	BER 2.4E-5

Note：all test condition compliance with IEEE P802.3cn™/D0.1

Electrical Characteristics

Table 5-Electrical Characteristics

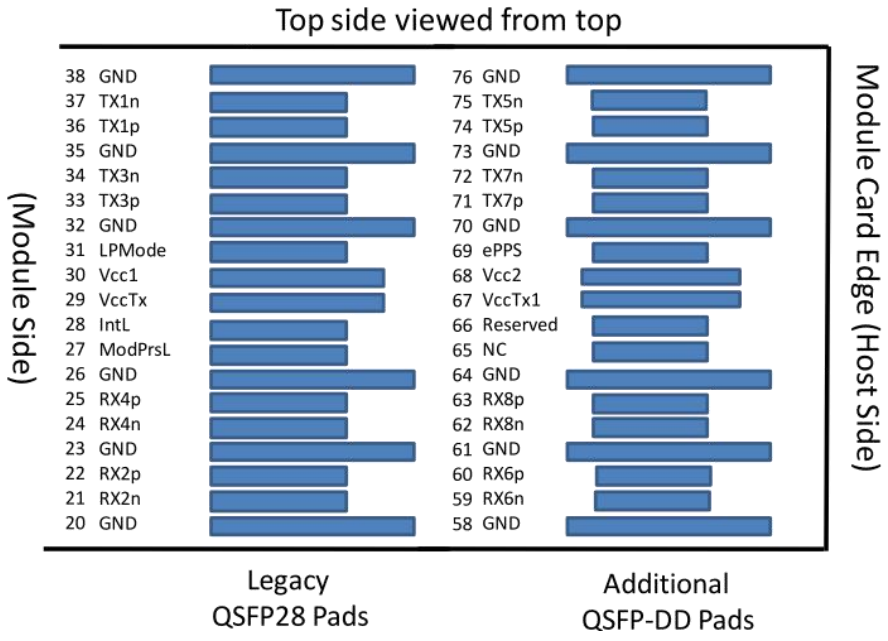
Transmitter (Module Input)						
Parameter		**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**
Differential Data Input Amplitude		$V_{IN,P-P}$	70	-	900	mVpp
Differential Termination Mismatch			-	-	10	%
Tx_Disable	Normal Operation	V_{IL}	-0.3	-	0.8	V
	Laser Disable	V_{IH}	2.0	-	V_{CC}+0.3	V
Receiver (Module Output)						
Parameter		**Symbol**	**Min.**	**Typical**	**Max.**	**Unit**
Differential Data Output Amplitude		$V_{OUT,P-P}$	200	-	900	mVpp
Differential Termination Mismatch（1MHZ）			-	-	10	%
Rx_LOS	Normal Operation	V_{OL}	-	-	0.4	V
	Lose Signal	V_{OH}	V_{CC}-0.5	-	V_{CC}+0.3	V

Digital Diagnostics

Table 6-Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	℃	Internal
Voltage	0 to V_{CC}	±3%	V	Internal
Tx Bias Current Per Lane	0 to 100	±10%	mA	Internal
Tx Output Power Per Lane	0.4 to 6.6	±3	dB	Internal
Rx Power (Each Lane)	LOS A to -2.4	±3	dB	Internal

Pin Definitions



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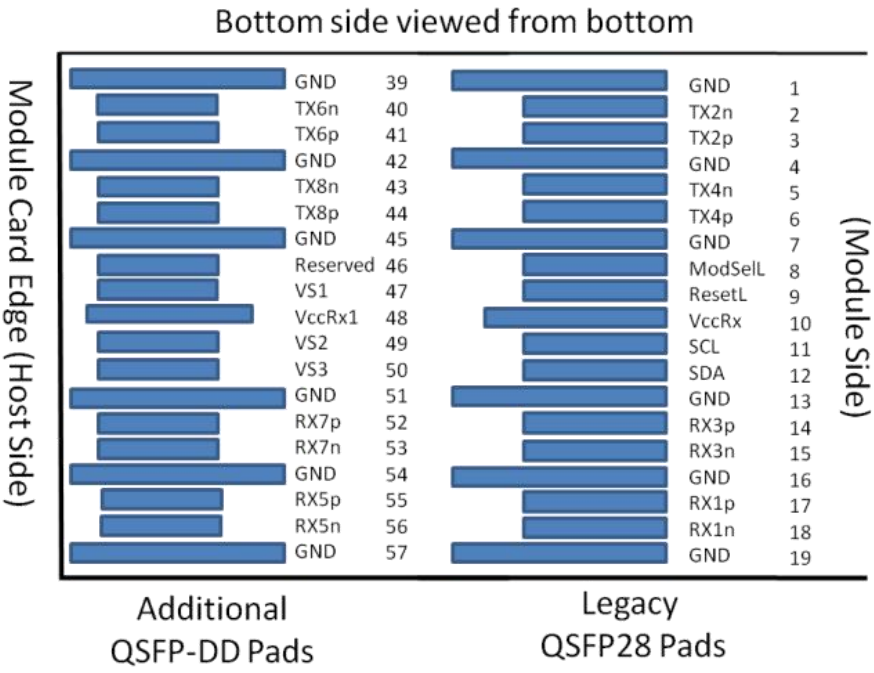


PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3B	
7		GND	Ground	1B	1
8	LVTLL-I	ModSelL	Module Select	3B	
9	LVTLL-I	ResetL	Module Reset	3B	
10		VccRx	+ 3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	

28	LVTTL-O	IntL/RX_LOS	Interrupt/Rx LOS	3B	
29		VccTx	+3.3 V Power Supply transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode/Tx_DIS	Low Power mode/Tx Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	

73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

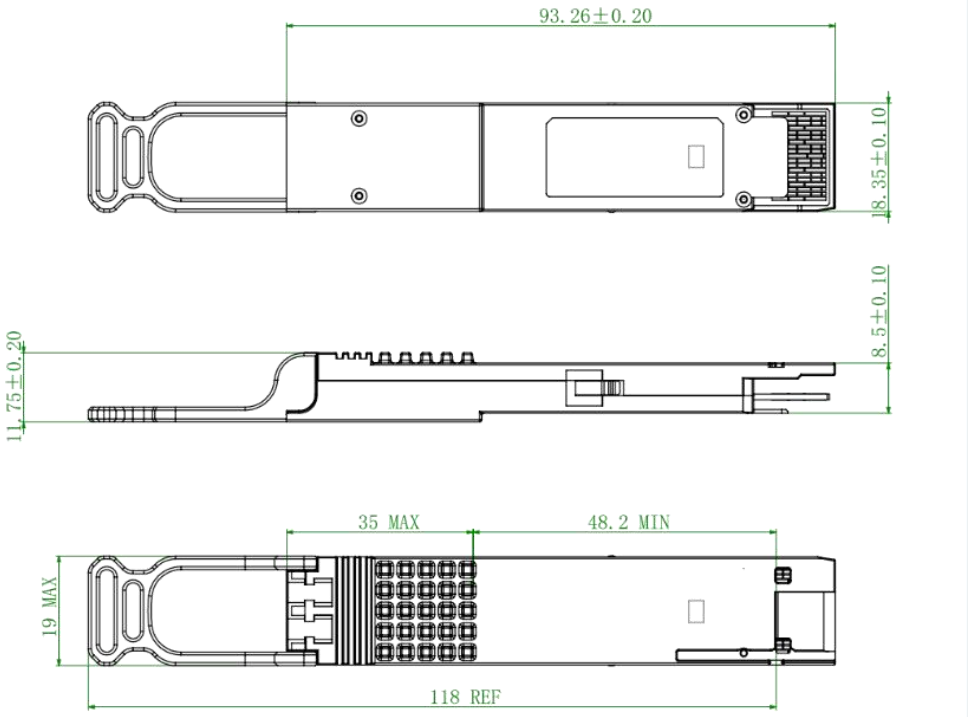
Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A,3B.

Mechanical Dimension



Warnings

Handling Precautions: This device is susceptible to damage as a result of electrostatic discharge (ESD). A static free environment is highly recommended. Follow guidelines according to proper ESD procedures.

Laser Safety: The WXTR# family Transceiver uses a semiconductor laser system and is a laser class1 product acc. FDA, complies with 21CFR1040. 10 and 1040.11. Also this product is a laser class 1 product acc. taclink